Hardware Implementation of 3-Phase Three Level Diode Clamped MLI Using SVPWM Technique

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Abstract: Multilevel inverters are increasingly being considered for high power applications because of their ability to get nearly a sinusoidal output voltage compared to normal two level inverters. Generally, there are three types of multilevel inverters, they are diode clamped, capacitor clamped, and cascaded multilevel inverters. The techniques generally used to generate the gating pulses are sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM). Among these two techniques, SVPWM is preferred because of its easy digitization and maximum dc bus voltage utilization. In this paper, the three phase three level diode clamped multilevel inverter (DCMLI) has been implemented using Space vector pulse width modulation technique (SVPWM). The gating pulses to the switches used in DCMLI are generated using this technique by writing the program in MPLAB software for the PIC microcontroller 18F452. The hardware setup and the experimental results are provided.

Keywords: Diode clamped multilevel inverter, Multilevel inerter, PIC microcontroller, Space vector pulse width modulation.

I. INTRODUCTION

The research on the multilevel inverter has been receiving wide attention mainly due to its capability of high voltage operation without switching devices connected in series. In addition, with the increase of voltage levels, the inverter output contains less harmonics and will eventually approach a desired sinusoidal waveform [1]. Therefore, the multilevel inverters have been selected as a preferred power converter topology for high voltage and high power applications [2], [3].

There are mainly three types of multilevel inverters. 1. Diode clamped multilevel inverter also called neutral point clamped multilevel inverter 2.Capacitor clamped multilevel inverter 3.Cascaded multilevel inverter.

Among all these, diode clamped multilevel inverter has some advantages, they are

1. High efficiency since fundamental switching frequency can be used for all devices
2. Controllable reactive power flow
3. Simple control method for back-to-back power transfer system

Besides these advantages, it has the following disadvantages.

1. High number of clamping diodes with high number of voltage levels
2. Difficulties with active power flow [4]
3. Capacitor Voltage Balance problem that need complex modulation

II. THREE LEVEL DIODE CLAMPED MULTILEVEL INVERTER

The fig. 1 represents the three level diode clamped multilevel inverter. The dc bus capacitor is divided into two, providing the neutral point Z. So each capacitor carries the half of the dc voltage. With a finite value for C_{n1} and C_{n2}, the capacitors can be charged or discharged by neutral current i, causing neutral point voltage deviation. The two diodes (D_{n1} and D_{n2}) connecting to the neutral point are called clamping diodes. There are 3 legs, each leg corresponding to each phase. Let us consider the leg A consists of 4 switches S_1 to S_4 as shown in fig 1. In general, IGBT or GCT is used as switches.

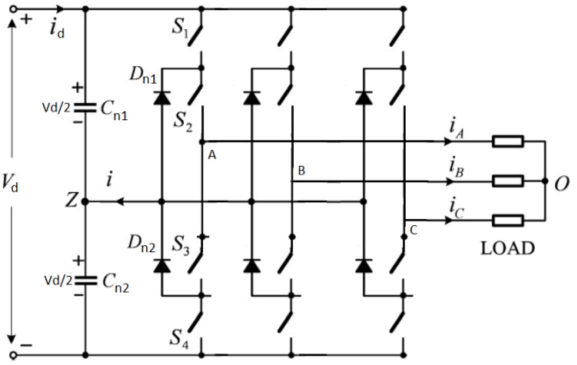

Fig. 1: Three level diode clamped multilevel inverter

Let P, O, and N are three possibilities of switching states in leg 1. Switching state P represents that the switches S_1 and S_2 are on, therefore the inverter terminal voltage is V_{AZ} which is equal to $V_d/2$. Similarly the other two switching states are also shown in table 1.

Table 1: Switching states

Switching State	Switches S1	 S2	 S3	 S4	Terminal voltage, V_{AZ}
P	on	on	off	off	$+V_d/2$
O	off	on	on	off	0
N	off	off	on	on	$-V_d/2$

III. SPACE VECTOR PULSE WIDTH MODULATION(SVPWM) TECHNIQUE

Space vector pulse width modulation (SVPWM) is one of the preferred real time modulation techniques and is widely used for digital control of voltage source inverters. This section presents the principle and implementation of the space vector modulation for 3 level DCMLI**.**

By considering all the three phases, there are total 27 possible switching states as shown in table 2. Among those 27 switching states, PPP, OOO, and NNN are called zero switching states and the others are called active switching states. All these switching states can be represented by space vectors. The typical space vector diagram for 3 level inverter is shown in fig. 2.

The relation between switching states and the space vectors can be derived as follows. Let us assume that the operation of the inverter is three phase balanced, then we have

$$v_{AO}(\mathrm{t}) + v_{BO}(\mathrm{t}) + v_{CO}(\mathrm{t}) = 0 \qquad (1)$$

Where v_{AO} , v_{BO} and v_{CO} are the instantaneous phase load voltages. From mathematical point of view, given any two phase voltages, the third one can be readily calculated. Therefore, it can be possible to transform the three phase variables to equivalent two phase variables.[6]

$$\begin{bmatrix} v_\alpha(\mathrm{t}) \\ v_\beta(\mathrm{t}) \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{AO}(\mathrm{t}) \\ v_{BO}(\mathrm{t}) \\ v_{CO}(\mathrm{t}) \end{bmatrix} \qquad (2)$$

A space vector can generally be represented by using the two variables in $\alpha - \beta$ plane as

$$V(\mathrm{t}) = v_\alpha(\mathrm{t}) + jv_\beta(\mathrm{t}) \qquad (3)$$

By substituting the equation(2) in the equation(3) , we get

$$\mathrm{V(t)} = \frac{2}{3}\left[v_{AO}(\mathrm{t})e^{j0} + v_{BO}(\mathrm{t})e^{j\frac{2\pi}{3}} + v_{CO}(\mathrm{t})e^{j\frac{4\pi}{3}} \right]$$

(4)

For active switching state POO, the generated load phase voltages are

$v_{AO}(\mathrm{t}) = \frac{1}{2}V_d$, $v_{BO}(\mathrm{t}) = 0$ and $v_{CO}(\mathrm{t}) = 0$

Substituting these values in equation(4), we get the corresponding space vector

$$V_{1P} = \frac{1}{3}V_d e^{j0}$$

Similarly we can calculate all the remaining vectors.

Table 2: Space vectors and switching states

Space vector		Switching State	Magnitude and phase
V_0		PPP, OOO, NNN	0
V_1	V_{1P}	POO	$\frac{1}{3}V_d e^{j0}$
	V_{1N}	ONN	
V_2	V_{2P}	PPO	$\frac{1}{3}V_d e^{j\frac{\pi}{3}}$
	V_{2N}	OON	
V_3	V_{3P}	OPO	$\frac{1}{3}V_d e^{j\frac{2\pi}{3}}$
	V_{3N}	NON	
V_4	V_{4P}	OPP	$\frac{1}{3}V_d e^{j\pi}$
	V_{4N}	NOO	
V_5	V_{5P}	OOP	$\frac{1}{3}V_d e^{j\frac{4\pi}{3}}$
	V_{5N}	NNO	
V_6	V_{6P}	POP	$\frac{1}{3}V_d e^{j\frac{5\pi}{3}}$
	V_{6N}	ONO	
V_7		PON	$\frac{\sqrt{3}}{3}V_d e^{j\frac{\pi}{6}}$
V_8		OPN	$\frac{\sqrt{3}}{3}V_d e^{j\frac{\pi}{2}}$
V_9		NPO	$\frac{\sqrt{3}}{3}V_d e^{j\frac{5\pi}{6}}$
V_{10}		NOP	$\frac{\sqrt{3}}{3}V_d e^{j\frac{7\pi}{6}}$
V_{11}		ONP	$\frac{\sqrt{3}}{3}V_d e^{j\frac{3\pi}{2}}$
V_{12}		PNO	$\frac{\sqrt{3}}{3}V_d e^{j\frac{11\pi}{6}}$
V_{13}		PNN	$\frac{2}{3}V_d e^{j0}$
V_{14}		PPN	$\frac{2}{3}V_d e^{j\frac{\pi}{3}}$
V_{15}		NPN	$\frac{2}{3}V_d e^{j\frac{2\pi}{3}}$

V_{16}	NPP	$\frac{2}{3}V_d e^{j\pi}$
V_{17}	NNP	$\frac{2}{3}V_d e^{j\frac{4\pi}{3}}$
V_{18}	PNP	$\frac{2}{3}V_d e^{j\frac{5\pi}{3}}$

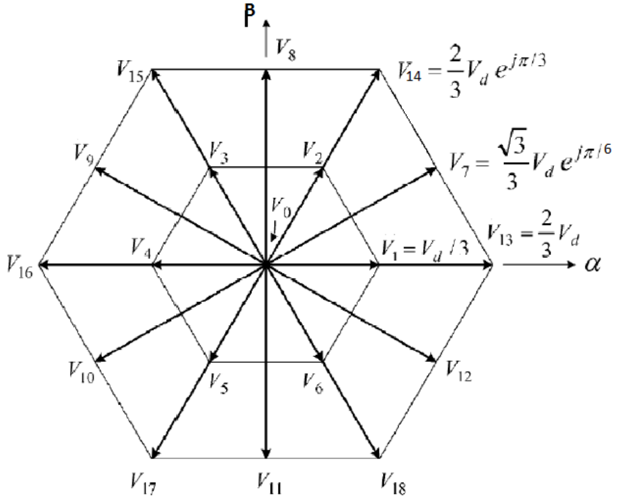

Fig. 2: Space vector diagram of a 3 phase inverter

All these zero and active vectors do not move in space. Let us assume a vector V_{ref} which rotates in space with an angular velocity ω as shown in fig. 3.

$$\omega = 2\pi f$$

Where f is the required output frequency, which means if the reference vector revolves one revolution then we will get one cycle of output voltage.

IV. DWELL TIME CALCULATION

To facilitate the dwell time calculation, the space vector diagram can be divided into 6 triangular sectors and each sector is divided into 4 triangular regions as shown in fig.3.

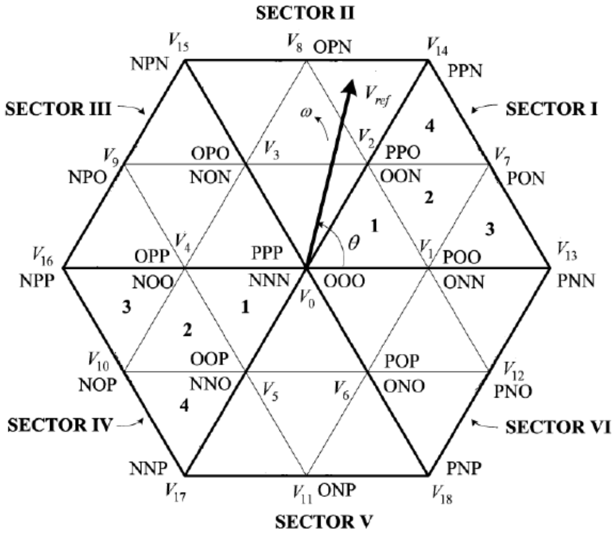

Fig. 3: Division of sectors and regions

The reference vector V_{ref} can be synthesized by three nearby stationary vectors. The dwell time for the stationary vectors represents the duty cycle time (on-state or off-state time) of the chosen switches during a sampling period T_s. The dwell time calculation is based on 'volt-second balancing' principle, that is, the product of V_{ref} and sampling period T_s equals the sum of the voltage multiplied by the time interval of chosen space vectors.
Now let us assume that the reference vector V_{ref} falls into region 2 of sector 1 as shown in fig 4.

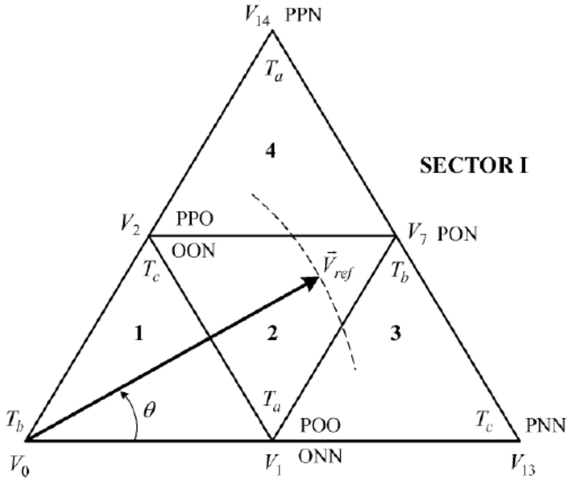

Fig. 4: Voltage vectors and their dwell times

The three vectors near to the reference vector are V_1, V_2 and V_7, from which

$$V_1T_a + V_7T_b + V_2T_c = V_{ref}T_s$$

And $T_a + T_b + T_c = T_s$

Where T_a,T_b and T_c are the dwell times for the vectors V_1, V_7 and V_2 respectively.
By substituting the voltage vectors

$V_1 = \frac{1}{3}V_d$, $V_2 = \frac{1}{3}V_d e^{j\frac{\pi}{3}}$, $V_7 = \frac{\sqrt{3}}{3}V_d e^{j\frac{\pi}{6}}$ and $V_{ref} = V_{ref}e^{j\theta}$ in the above equations and solve for T_a, T_b and T_c, we get

$$T_a = T_s\left[1 - 2m_a \sin\theta\right]$$

$$T_b = T_s\left[2m_a \sin\left(\frac{\pi}{3} + \theta\right) - 1\right]$$

And $$T_c = T_s\left[1 - 2m_a \sin\left(\frac{\pi}{3} - \theta\right)\right]$$

For $0 \le \theta \le \frac{\pi}{3}$

Where m_a is called modulation index and is defined as

$$m_a = \frac{\sqrt{3}V_{ref}}{V_d}$$

Similarly we can calculate the dwell times for the switching states corresponding to in which region the reference vector falls.

V. SWITCHING SEQUENCE DESIGN

The requirements in designing the switching sequence are as follows.

1. The transition from one switching state to the other should involve only two switches, one being turned on and the other being turned off.
2. The transition for V_{ref} from one sector (or region) to the next sector (or region) should require no or minimum number of switchings.
3. The voltage between the neutral point (Z) and the negative dc bus is called the neutral point voltage V_z, which varies with the switching state. We should minimize the effect of switching state on the neutral point voltage deviation.

VI. EFFECT OF SWITCHING STATE ON THE NEUTRAL POINT VOLTAGE DEVIATION

Let us assume that the vectors having the length $\frac{1}{3}V_d$ are small vectors, $\frac{\sqrt{3}}{3}V_d$ are medium vectors and $\frac{2}{3}V_d$ are large vectors.

There are P-type and N-type vectors in small vectors as shown in the table 2.

1. Zero vectors do not affect the neutral point voltage.
2. P-type small vectors make V_z to rise and N-type small vectors make V_z to decline.
3. Medium vectors also affect V_z, but the direction of voltage change is undefined.
4. Large vectors like zero vectors do not affect V_z.[7]

So while designing the switching sequence, to minimize the neutral point voltage deviation, the dwell times of p-type and N-type vectors should be equally distributed.

According to the region that the reference vector lies in, the following two cases can be considered.

A. One small vector in three selected vectors

When the reference vector lies in region 3 or 4 of sector 1, then we have only one small vector among 3 selected vectors. Let us assume that the reference vector lies in region 3, and then the selected vectors are V_1, V_7 and V_{13}. Among these three, V_1 is the only small vector. The small vector V_1 has two switching states POO and ONN. To minimize the neutral voltage deviation, the dwell time for V_1 should be equally distributed between the P- type and N-type switching states. Assuming the dwell times for V_1, V_7 and V_{13} are T_c, T_a, and T_b respectively, the typical switching sequence is shown in fig. 5.

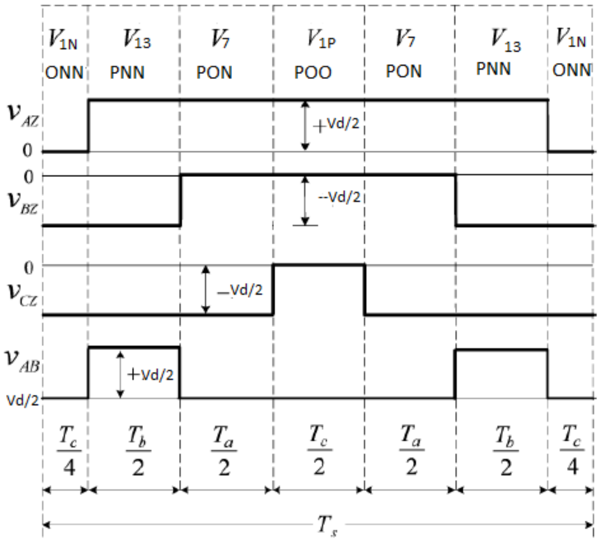

Fig 5: switching sequence for V_{ref} in sector I region 3

B. Two small vectors in three selected vectors

When V_{ref} is in region 1 or 2 of sector 1, two of the three selected vectors are small vectors. To reduce the neutral point voltage deviation, each of the two regions is further divided into two sub regions as shown in Fig 6. Assuming that V_{ref} lies in region2a, it can be synthesized by V_1, V_2, and V_7. Since V_{ref} is closer to V_1 than V_2, the corresponding dwell time T_a for V_1 is longer than T_c for V_2. The vector V_1 is referred to as dominant small vector, whose dwell time is equally divided between V_{1P} and V_{1N} as shown in Table 3.[7]

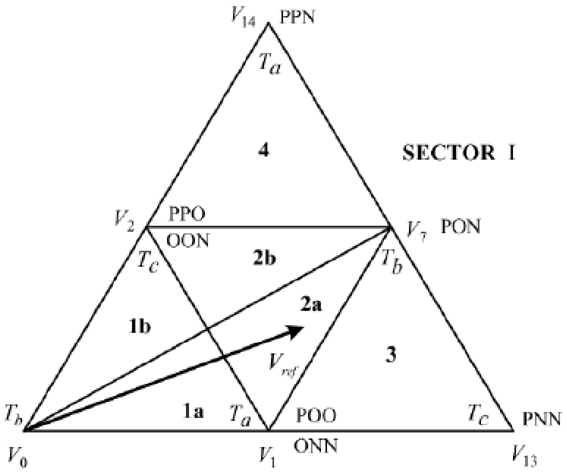

Fig. 6: Division of six regions of sector I for the minimization of neutral point voltage deviation.

Table. 3: Switching sequence for V_{ref} in sector I region 2a

Voltage vector	V_{1N}	V_{2N}	V_7	V_{1P}	V_7	V_{2N}	V_{1N}
Switching state	O N N	O O N	P O N	P O O	P O N	O O N	O N N
Dwell time	$\frac{Ta}{4}$	$\frac{Tc}{2}$	$\frac{Tb}{2}$	$\frac{Ta}{2}$	$\frac{Tb}{2}$	$\frac{Tc}{2}$	$\frac{Ta}{4}$

VII. HARDWARE IMPLEMENTATION AND WAVEFORMS

The specifications used in writing the program are as follows

Modulation index, ma=0.7
Sampling period, Ts=0.667ms
Sampling Frequency, fsp=1.5kHz
Frequency of output voltage=50 Hz

The hardware setup is shown below

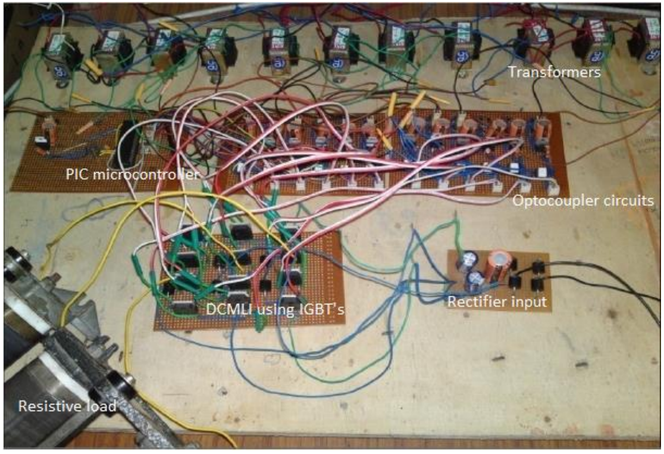

Fig. 7: Hard ware setup

We have given an input voltage of 50V to the inverter, therefore the voltage V_{AB} in fig. 9 shows maximum voltage of 50V and the voltage V_{AZ} in fig. 10 shows maximum of 25(I,e $V_d/2$) volts.

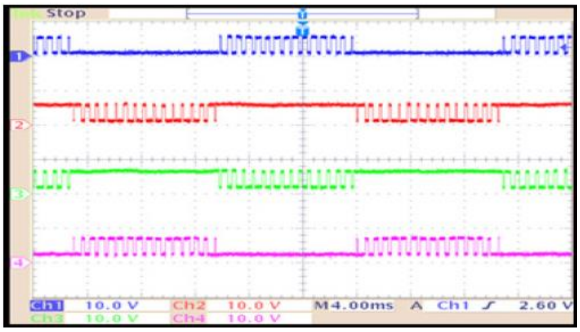

Fig. 8:The gating pulses to the four switches in leg1

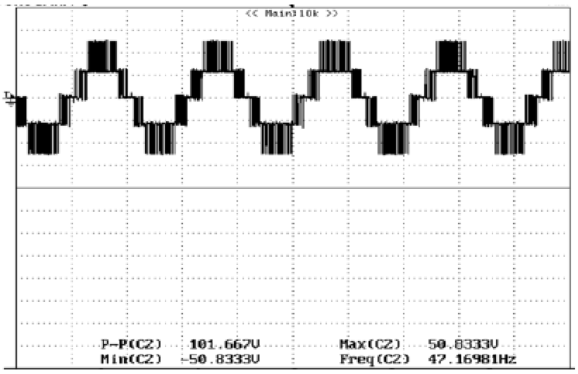

Fig. 9: Voltage V_{AB}

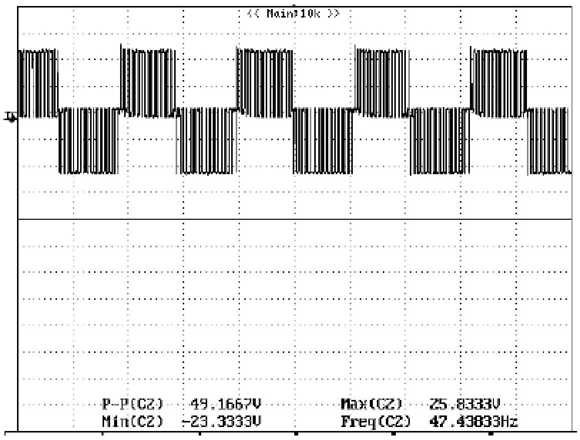

Fig 10: Voltage V_{AZ}

VIII. RESULT

In this paper, Space vector pulse width modulation technique has been explained and is applied to three phase three level diode clamped multilevel inverter. The program corresponding to SVPWM technique is written in PIC18f452 by using the specifications mentioned above to generate the gating pulses to the switches. The output voltage waveform and other waveforms are shown.

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